BLF8G24L-200P; BLF8G24LS-200P

Power LDMOS transistor

Rev. 3 — 12 July 2013 Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 2300 MHz to 2400 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2300 to 2400	1740	28	60	17.2	32	−37 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

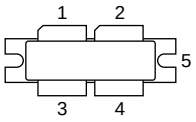
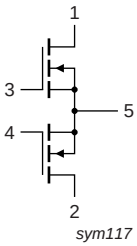
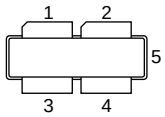
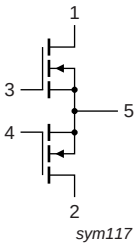
- Excellent ruggedness
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF8G24L-200P (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF8G24LS-200P (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G24L-200P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF8G24LS-200P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C
T_{case}	case temperature	[1]	-	150	°C

[1] Continuous use at maximum temperature will affect the MTTF.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 60 W	0.217	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 100 mA	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	26.8	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5.1 A	-	1.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.04 A	-	0.1	-	Ω

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA, PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 64 DPCH; f_1 = 2300 MHz; f_2 = 2400 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1740 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	60	-	W
G_p	power gain		15.8	17.2	-	dB
RL_{in}	input return loss		-	–11	–8	dB
η_D	drain efficiency		27	32	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)		-	–37	–33	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G24L-200P and BLF8G24LS-200P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1740 mA; P_L = 200 W (CW); f = 2300 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data half section; V_{DS} = 28 V; I_{Dq} = 860 mA; typical values unless otherwise specified.

f	Z_S[1]	Z_L[1]
(MHz)	(Ω)	(Ω)
2300	4.24 – j6.5	1.5 – j5.4
2400	7.47 – j6.07	1.5 – j5.5

[1] Z_S and Z_L defined in Figure 1.

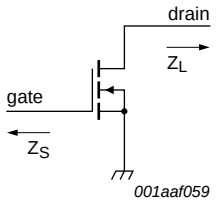
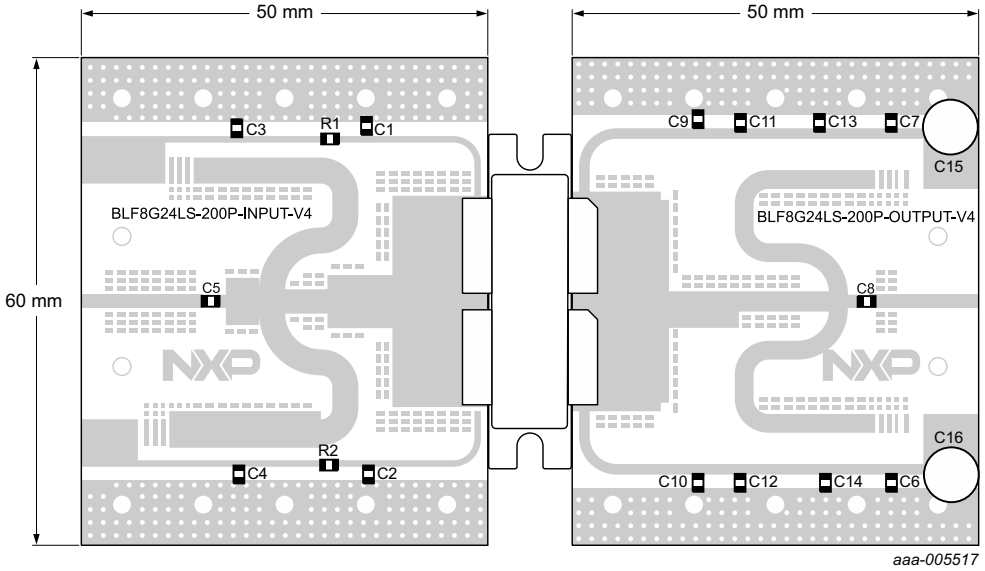


Fig 1. Definition of transistor impedance

7.3 Test circuit



See Table 9 for list of components.

Fig 2. Component layout

Table 9. List of components

See Figure 2 for component layout.

The used PCB material is Rogers RO4350B with a thickness of 0.76 mm.

Component	Description	Value	Remarks
C1, C2, C9, C10	multilayer ceramic chip capacitor	6.8 μF	[1]
C3, C4, C6, C7	multilayer ceramic chip capacitor	1 μF	[2]
C5, C8	multilayer ceramic chip capacitor	33 pF	[1]
C11, C12, C13, C14	multilayer ceramic chip capacitor	0.1 μF	[2]
C15, C16	electrolytic capacitor	1000 μF; 50 V	
R1, R2	chip resistor	5.1 Ω	[3]

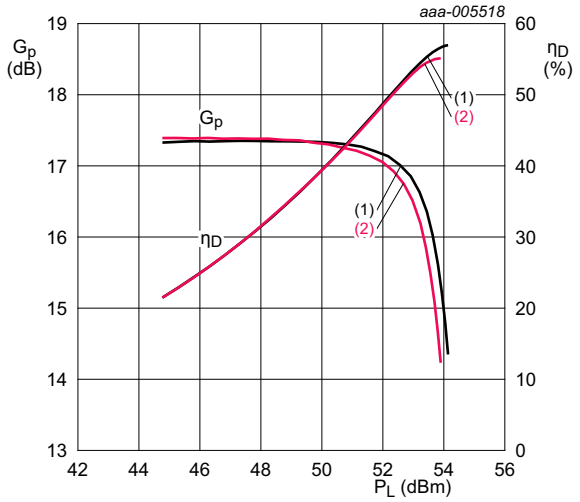
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] Murata or capacitor of same quality.

[3] Vishay Dale or resistor of same quality.

7.4 Graphical data

7.4.1 1-Tone CW



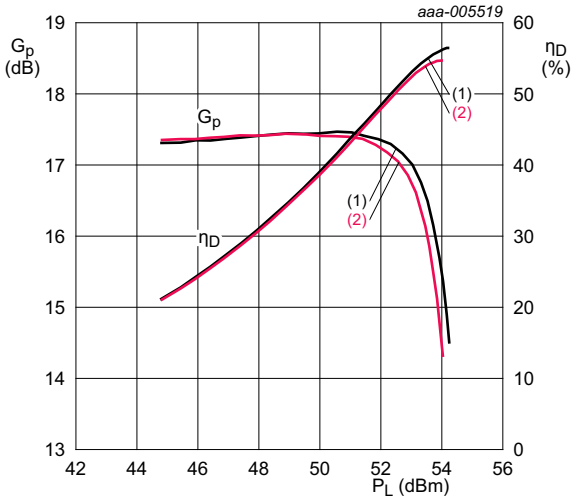
V_{DS} = 28 V; I_{Dq} = 1740 mA.

(1) f = 2300 MHz

(2) f = 2400 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values

7.4.2 1-Tone CW pulsed



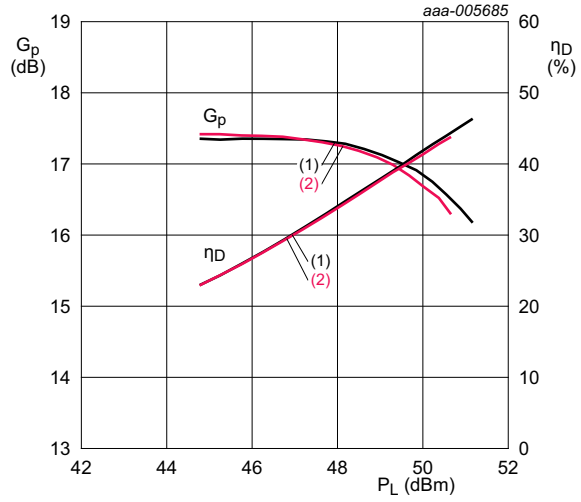
V_{DS} = 28 V; I_{Dq} = 1740 mA.

(1) f = 2300 MHz

(2) f = 2400 MHz

Fig 4. Power gain and drain efficiency as function of load power; typical values

7.4.3 1-Carrier W-CDMA

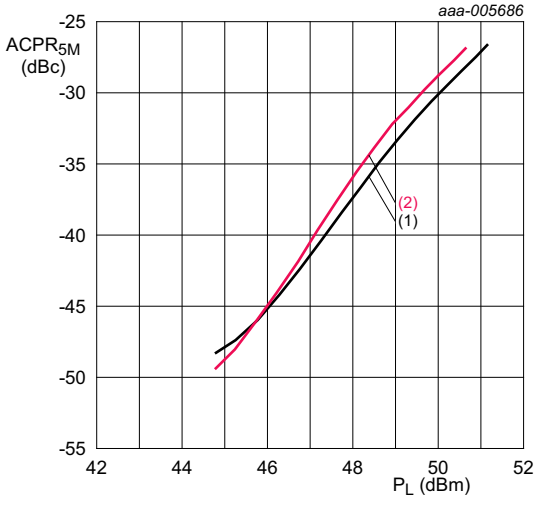


V_{DS} = 28 V; I_{Dq} = 1740 mA.

(1) f = 2300 MHz

(2) f = 2400 MHz

Fig 5. Power gain and drain efficiency as function of load power; typical values

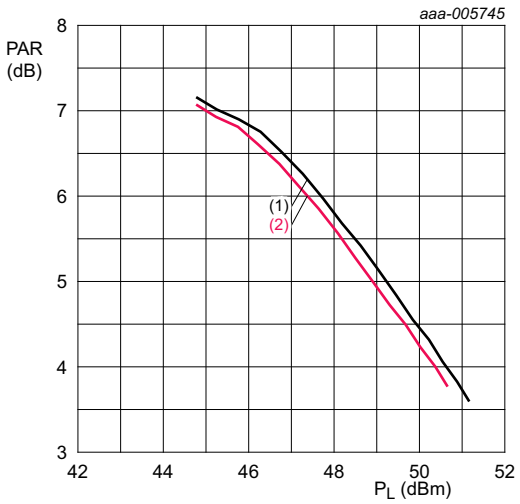


V_{DS} = 28 V; I_{Dq} = 1740 mA.

(1) f = 2300 MHz

(2) f = 2400 MHz

Fig 6. Adjacent power channel ratio (5 MHz) as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 1740 mA.

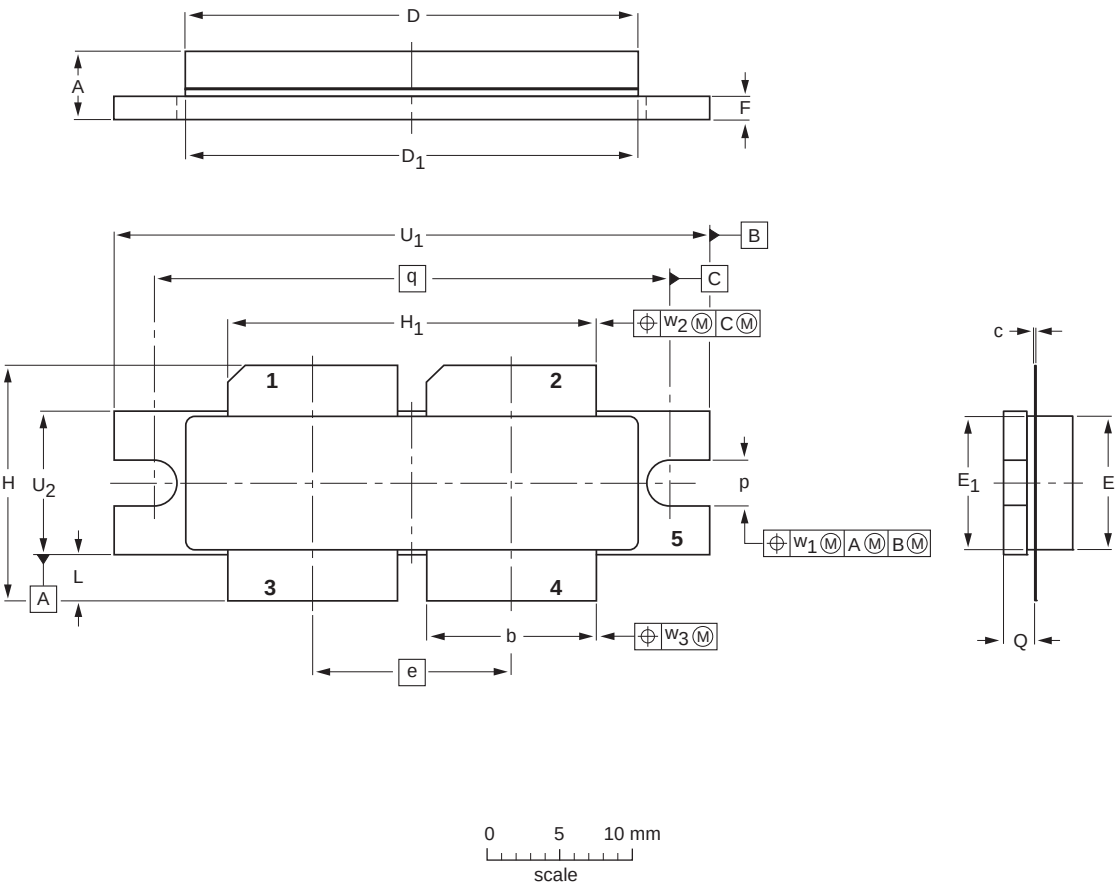
(1) f = 2300 MHz

(2) f = 2400 MHz

Fig 7. Peak-to-average power ratio as a function of load power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

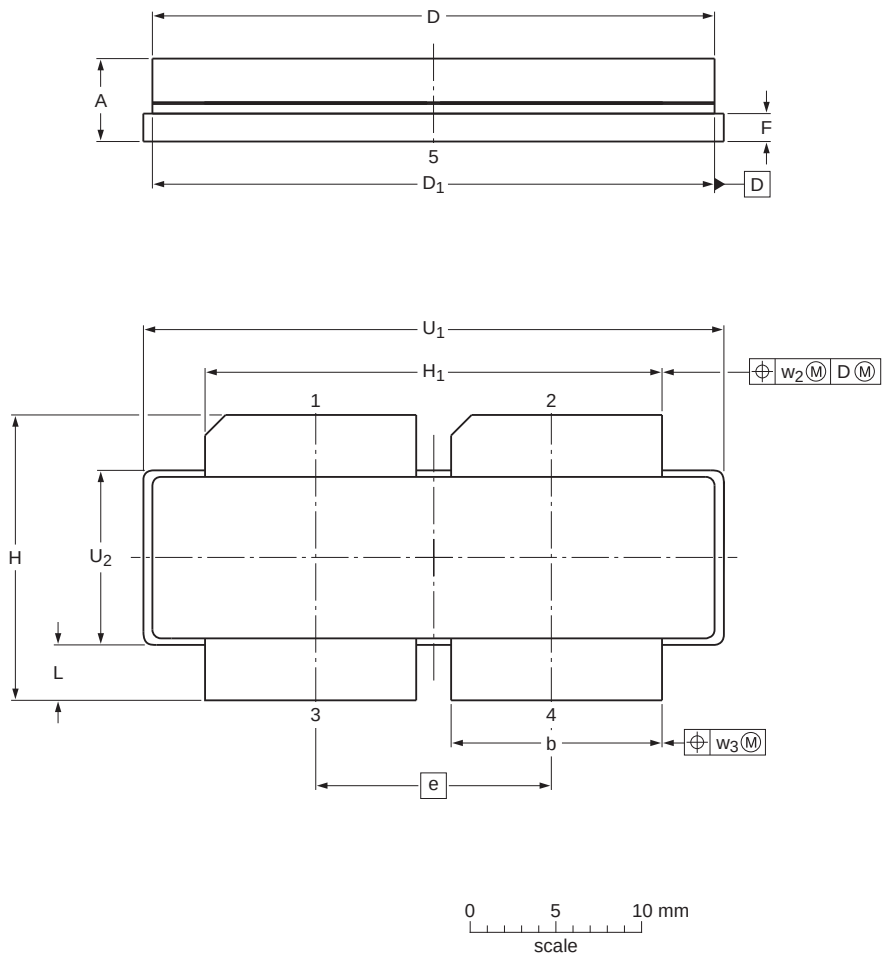
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 8. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 9. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
DPCH	Dedicated Physical Channel
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTTF	Mean Time To Failure
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G24L-200P_LS-200P v.3	20130712	Product data sheet	-	BLF8G24L-200P_LS-200P v.2
Modifications:	• The package outline Figure 9 is updated.			
BLF8G24L-200P_LS-200P v.2	20121203	Product data sheet	-	BLF8G24L-200P_LS-200P v.1.1
Modifications:	• Table 1 on page 1: several changes. • Table 4 on page 2: several changes. • Table 5 on page 3: added typical value. • Table 6 on page 3: changed several values. • Table 7 on page 3: several changes. • Table 7 on page 3: table moved to.Section 6 • Section 7.1 on page 3: changed the value of I_{Dq}. • Section 7.2 on page 4: added section. • Section 7.3 on page 4: added section. • Section 7.4 on page 5: added section. • Section 9 on page 10: added section.			
BLF8G24L-200P_LS-200P v.1.1	20120220	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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